AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF THE CLAIMS:

1. (Currently Amended) A microprocessor built on a semiconductor chip comprising:

a central processing unit for executing instructions and generating address signals;

an external bus interface control circuit, coupled to said central processing unit via an internal bus, which controls an external bus based on execution of instructions by said central processing unit, said external bus interface control circuit being capable of ~~selecting~~ activating one of a plurality of external device select signals corresponding to said address signals, ~~an external access address and activating said selected external device select signal~~ said external device select signals being output from said microprocessor;

a clock generating circuit, coupled to said central processing unit ~~and said external bus interface control circuit~~, to generate a plurality of clock signals including a first clock signal and a second clock signal;

a clock switching control circuit for controlling an operation to switch a synchronous clock signal ~~provided~~

providing one of said first clock signal and said second clock signal to said external bus interface control circuit in accordance with said external device select signal ~~activated by said external bus interface control circuit~~;

a first clock terminal~~, coupled to said clock generating circuit,~~ to supply [[a]] said first clock signal to a first external device; and

a second clock terminal~~, coupled to said clock generating circuit,~~ to supply [[a]] said second clock signal to a second external device, ~~in parallel with said first clock signal,~~

wherein said second clock signal ~~having~~ has a different frequency from said first clock signal, and said first and second clock signals are output from said microprocessor to said first and second external devices, respectively, in parallel.

2. (Currently Amended) A microprocessor comprising:

a central processing unit for executing instructions and generating at least one external access address; and

an external bus interface control circuit which controls an external bus based on execution of instructions by said central processing unit,

wherein said external bus interface control circuit is capable of activating either a first external device select signal or a second external device select signal corresponding to ~~an~~ said external access address,

wherein said microprocessor includes a clock switching control circuit and a clock pulse generator,

wherein said clock switching control circuit controls an operation to switch a synchronous clock signal of said external bus interface control circuit to one of a first clock signal in accordance with activation of said first external device select signal [[or to]] and a second clock signal in accordance with activation of said second external device select signal,[[and]]

wherein said clock pulse generator generates said first clock signal and said second clock signal, [[and]] said first clock signal [[is]] having a predetermined frequency different from that of said second clock signal, and

wherein said microprocessor includes first and second external clock output terminals outputting said first and second clock signals, respectively, in parallel.

3-5 (Canceled).

6. (Currently Amended) The microprocessor according to claim 2,

wherein said clock switching control circuit requests said central processing unit to suspend execution of instructions in response to activation of a selected external device select signal, and

wherein said clock switching control circuit is further capable of switching said synchronous clock signal, which is provided to said external bus interface control circuit, after an acknowledgment of the request to suspend instruction execution.

7. (Currently Amended) The microprocessor according to claim 6, wherein said clock switching control circuit is capable of switching ~~said~~ a clock signal of said central processing unit in accordance with switching said synchronous clock signal of said external bus interface control circuit.

8-14 (Canceled).